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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,506	02/11/2002	David Chow	42390P11248	7439

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EXAMINER	
DUNCAN, MARC M	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,506	CHOW ET AL.	
	Examiner	Art Unit	
	Marc M Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19* is/are rejected.

7)☒ Claim(s) *18 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

Claims 1-17 and 19 are rejected under 35 U.S.C. 103(a).

Claims 5-8 are rejected under 35 U.S.C. 101.

Claims 18 and 20-22 are objected to.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 5-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The storage medium of claims 5-8 is not a computer readable medium.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 2, 4, 5, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Dorsey.

Regarding claim 1:

Nakamura teaches loading a value into a register of a memory device in col. 3 lines 13-16.

Nakamura teaches generating a test sequence in response to the value in the register during a self-test mode of operation of the memory device in col. 3 lines 13-16 and lines 43-45.

Nakamura teaches testing the memory device with the test sequence in the entire document.

Nakamura does not explicitly teach storing a signature as a result of the test sequence into a shift register. Nakamura does, however, teach storing output data.

Dorsey teaches storing a signature as a result of the test sequence into a shift register in paragraph 0009 lines 7-9 and paragraph 0042 lines 2-4.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the signature register of Dorsey with the output storing of Nakamura.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the storing of the signature as taught by Dorsey allows the output to be analyzed off chip using conventional JTAG or other methods.

Regarding claim 2:

Nakamura teaches wherein the value is a four bit field in col. 6 lines 52-56. In order for the counter to represent number 8-11, there would have to be four bits.

Regarding claim 4:

Nakamura teaches wherein the test sequence is one of a test pattern or a plurality of test patterns in col. 3 lines 43-45.

Regarding claim 5:

The claim is rejected as the computer readable medium with computer executed instructions that, when executed, perform the method of claim 1.

Regarding claim 6:

The claim is rejected as the computer readable medium with computer executed instructions that, when executed, perform the method of claim 2.

Regarding claim 8:

The claim is rejected as the computer readable medium with computer executed instructions that, when executed, perform the method of claim 4.

Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Dorsey as applied to claims 1 and 5 above, and further in view of Perner et al.

Regarding claims 3 and 7:

The teachings of Nakamura and Dorsey are outlined above.

Nakamura and Dorsey do not explicitly teach the memory device being a polymer memory. Nakamura and Dorsey do, however, teach a memory.

Perner teaches a memory device being a polymer memory in col. 1 lines 22-23.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the polymer memory of Perner with the BIST teachings of Nakamura and Dorsey.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because polymer memory is high density, low voltage, fast and cost efficient.

The teachings of Nakamura, Dorsey and Perner do not explicitly teach the memory being an 8K by 8K array with a 256 bit data word. Nakamura, Dorsey and Perner do, however, teach a memory.

The examiner takes official notice that the use of an 8K by 8K array with a 256 bit data word was well known to those of ordinary skill in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the 8K by 8K array with a 256 bit data word with the memory of Nakamura, Dorsey and Perner.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because sizing of data arrays in memory devices was well-known and widely used to meet a specific storage requirement. The use of a 256 bit data word is a common occurrence because data words in computer memories are sized in powers of 2, and 256 is equal to 2 to the power of 8.

Claims 9, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Dorsey as applied to claim 1 above, and further in view of Schwarz.

Regarding claim 9:

The teachings of Nakamura and Dorsey are outlined above.

Nakamura and Dorsey do not explicitly teach an error counter. Nakamura and Dorsey do, however, teach detecting error in a memory using a BIST.

Schwarz teaches an error counter to tabulate the number of errors as the result of the test sequence in col. 3 lines 56-59.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the error counter of Schwarz with the BIST of Nakamura and Dorsey.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the use of the error counter allows the tester to determine when the memory has to many errors to be useable.

Regarding claim 10:

Nakamura teaches wherein the value is a four bit field in col. 6 lines 52-56. In order for the counter to represent number 8-11, there would have to be four bits.

Regarding claim 12:

Nakamura teaches wherein the test sequence is one of a test pattern or a plurality of test patterns in col. 3 lines 43-45.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, Dorsey and Schwarz as applied to claim 9 above, and further in view of Perner.

Regarding claim 11:

The teachings of Nakamura, Dorsey and Schwarz are outlined above.

Nakamura, Dorsey and Schwarz do not explicitly teach the memory device being a polymer memory. Nakamura, Dorsey and Schwarz do, however, teach a memory.

Perner teaches a memory device being a polymer memory in col. 1 lines 22-23.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the polymer memory of Perner with the BIST teachings of Nakamura, Dorsey and Schwarz.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because polymer memory is high density, low voltage, fast and cost efficient.

The teachings of Nakamura, Dorsey, Schwarz and Perner do not explicitly teach the memory being an 8K by 8K array with a 256 bit data word. Nakamura, Dorsey and Perner do, however, teach a memory.

The examiner takes official notice that the use of an 8K by 8K array with a 256 bit data word was well known to those of ordinary skill in the art at the time of invention.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the 8K by 8K array with a 256 bit data word with the memory of Nakamura, Dorsey, Schwarz and Perner.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because sizing of data arrays in memory devices was well-known and widely used to meet a specific storage requirement. The use of a 256 bit data word is a common occurrence because data words in computer memories are sized in powers of 2, and 256 is equal to 2 to the power of 8.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, Dorsey and Schwarz as applied to claim 9 above, and further in view of Katz.

Regarding claim 13:

The teachings of Nakamura, Dorsey and Schwarz are outlined above.

Nakamura, Dorsey and Schwarz do not explicitly teach the counter utilizing a shift register to tabulate the number of errors.

Katz teaches a shift register utilized as a counter on page 353 lines 7-14.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the shift register counter of Katz with the counter of Nakamura, Dorsey and Schwarz.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the counter of Katz is synchronous (see page 354 lines 8-9).

Claims 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Schwarz.

Regarding claim 14:

Kim teaches a logic to support programmable built-in self-test patterns in Fig. 1.

Kim does not explicitly teach an error counter to tabulate a number of errors detected as a result of at least one BIST pattern applied to the memory device. Kim does, however, teach detecting errors to determine the functionality of a memory device.

Schwarz teaches an error counter to tabulate the number of errors as the result of the test sequence in col. 3 lines 56-59.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the error counter of Schwarz with the BIST of Kim.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the use of the error counter allows the tester to determine when the memory has to many errors to be useable.

Regarding claim 15:

Kim teaches a plurality of programmable input data to test the memory device in paragraph 0014 lines 7-8 and lines 11-12.

Regarding claim 16:

Kim teaches wherein at least one BIST pattern is to be generated by a data pattern stored in a chip test data register based at least in part on an address of the memory in paragraph 0031 lines 4-6.

Regarding claim 17:

Schwarz teaches wherein the error counter is reset to zero before the BIST pattern is applied to the memory device in col. 4 line 4.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Schwarz as applied to claim 14 above, and further in view of Hii et al.

Regarding claim 19:

The teachings of Kim and Schwarz are outlined above.

Kim and Schwarz do not explicitly teach wherein the error counter is to count errors for a subset of the memory device, defined by a starting address and an ending address. Kim and Schwarz do, however, teach an error counter for counting errors of a memory device.

Hii teaches wherein the error counter is to count errors for a subset of the memory device, defined by a starting address and an ending address in the Abstract line 5-13.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the starting and ending address of Hii with the error counter of Kim and Schwarz.

One of ordinary skill in the art at the time of invention would have been motivated to combine the teachings because the use of starting and ending addresses allows for only a subarray of the memory unit to be tested.

Allowable Subject Matter

Claims 18 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests wherein the error counter is incremented if the errors exceed a programmable threshold for an address as outlined in claim 18. Prior art was not found that explicitly teaches or fairly suggests wherein the error counter is to count errors for a subset of a word as outlined

in claim 20. Prior art was not found that explicitly teaches or fairly suggests wherein the error counter is a plurality of registers, the registers to store a count for at least one defect type and to store a count of the number of good bits for an address as outlined in claim 21. These limitations are considered allowable only in combination with the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art not relied upon contains elements of the instant claims and/or represents a current state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc M Duncan whose telephone number is 703-305-4622. The examiner can normally be reached on M-T and TH-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 703-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

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